Frequently Asked Questions about CALCE Electronic Products and Systems Consortium Membership

1. What are the different levels of membership in the CALCE Consortium?

A CALCE Consortium membership is given only to a designated site of a sponsoring organization. A designated site is an agreed upon geographical location of an organization where employees of the organization work and where access to CALCE Center resources is provided. Employees at each designated site can have access to CALCE Center resources and can attend the biannual CALCE Consortium Technical Review and Planning Meetings.

There are four types of CALCE Consortium Members. These are:

Super Member - $125,000 per year
Full Member - $65,000 per year
Associate Member - $30,000 per year
Site Member - $15,000 per year

Full membership has one designated site and additional site members can be added. Super members are not charged for additional sites. Associate Membership is available only to companies with less than 250 employees.

Super and Full members can submit research proposals to CALCE Center investigators for consideration in the development of formal CALCE Consortium Research Projects. Site members have access to CALCE Center Resources and may work with Full members to develop research projects.

2. What resources are available to consortium members?

CALCE Consortium members can participate and receive information on every CALCE Consortium project and access the CALCE Web Site, which contains:

CALCE Software

- *CalcePWA* – A virtual qualification package for evaluating circuit card assemblies (printed circuit board assemblies, or printed wiring board assemblies)
- *CADMP-II* - A virtual qualification package for evaluating package electronic devices (MCM, integrated circuits)
- *CalceFAST* – A failure assessment package which provides access to failure models for solder interconnects, plated through hole vias, and other device package failures.
- *CalceFAST-On-Line* – A web based version of calceFAST.

CALCE Web Resources - including

- *Accelerated Product Qualification and Quality Assurance* - This online resource presents interactive physics-of-failure guidelines for accelerated product qualification and quality assurance. The material is intended to give electronics manufacturers, suppliers, managers, analysts, and engineers a rational understanding of efficient ways to assess product durability and quality. Further, the fundamental concepts required to develop a successful physics-of-failure based accelerated qualification and quality assurance program that meets the product requirements, lowers life-cycle costs and reduces the time-to-market are addressed in detail through interactive case-studies. The valuable lessons learned are outlined as a set of generic guidelines to help design, plan, and implement a PoF based accelerated qualification program.

- *Circuit Card Assemblies Failure Mechanism Handbook* - The CALCE CCA Failure Mechanism Handbook is an evolving technology that is intended to allow design engineers, product managers, reliability analysts, and failure analysts to rapidly evaluate failure risks for circuit card assemblies (CCA). This resource describes, compares, and critiques different failure models for CCAs. Examples include thermomechanical fatigue, vibration fatigue, mechanical shock/warpage damage, and chemical/corrosion damage. Access to online failure calculators is also provided.
- *Contract Assembly Assessment* - The growth in popularity of contract assembly outsourcing in the electronics industry and the absence of concrete procedures for the outsourcing process form the motivation for this research work. Contract outsourcing involves the transfer of specific assembly activities related to a product or process from an OEM (Original Equipment Manufacturer) to a CA (Contract Assembler). This web site presents industry outsourcing data from the top OEMs and CAs, step-by-step procedures for performing benchmarking and the management of the CA, the economics of outsourcing, and several case studies of large OEMs that have successfully performed outsourcing of electronics assembly activities.
- *Electronic Packaging Materials and Their Properties* - A source for properties of materials at all levels of electronic packaging. Fully updated from first edition. This webbook reviews the key electrical, thermal and thermomechanical, mechanical, chemical, and miscellaneous properties and their significance in electronic packaging.
- *Escape Routing and Footprint Analysis* - A limiting requirement for some parts is escape routing. If a part's I/O are in an area array format (as opposed to peripherally bonded), the part can not be wired into the system until all of its I/O are routed out from under the part. This situation is encountered for flip chip bonded die and die in various array format chip scale packages such as BGAs (Ball Grid Arrays). The process of liberating I/O from an array is called escape routing. If the array is small enough (small I/O count), or the line width and line spacing in the board is fine enough, it may be possible to escape all the I/O on the top layer of the board. More often, however some I/O must use vias to drop to other layers to be escape routed. If additional layers must be used, the combination of the part I/O pitch and connection size, and the via and/or hole capture pad sizes must allow the placement of a via or hole capture on the board within the part I/O array, or it is impossible to drop unescaped I/O to deeper layers. In addition, many board technologies, especially microvia Printed Wiring Boards (PWBs), have practical limitations on the number of layers that can be fabricated. A part that requires too many layers to escape route may have to be rejected. This tool can be used to: 1) Determine whether a specific part can be escape routed when interconnected to a specific board technology, and 2) Determine the footprint occupied by the part on the top layer of the board.
- *Guidebook for Managing Silicon Chip Reliability* - This resource describes the principal failure mechanisms associated with modern IC's, and the typical practices used to address them. This book focuses on the individual failure mechanisms associated with semiconductor devices. A list of failure sites, operational loads, and failure mechanisms associated with semiconductor devices is provided. This webbook discusses topics such as intrinsic device sensitivities, electromigration, hot-carrier aging, time-dependent dielectric breakdown, mechanical stress induced migration, alpha particle sensitivity, electrostatic discharge (ESD) and electrical overstress, and latchup. This webbook presents some guidelines for designing for reliability, process development and qualification issues, and provides insight into screening.
- *High Temperature Electronic Packaging* - This interactive guidebook for the development of electronic systems for use at temperatures above 125 °C provides information for each package element. Information includes material properties, failure mechanisms, failure models, and manufacturing sites.
- *Influence of Temperature on Microelectronics and System Reliability* - An authoritative source on the effects of temperature on microelectronic device failure mechanisms. The document

covers the important issues of steady state temperature dependent models, temperature effects associated with temperature cycling, temperature gradient, and time dependent temperature changes. It identifies models quantifying the temperature effects on various package elements and addresses the impacts of various design-for-temperature trade-offs on electronic systems. Temperature related models are assessed in terms of their use for determining the maximum and minimum allowable thermal stresses for a given system architecture

- *Integrated Circuit, Hybrid and MCM Package Design Guidelines* – This handbook provides descriptions of critical failure mechanisms for a wide range of packaging elements in IC, hybrid and multi-chip module packages. It also gives fundamental models for assessing the susceptibility for failure of these electronic products.
- *Integral Passives* - This resource provides an introduction to Integral Passives (IPs). The resource covers materials, economics, and failure issues related to using Ips. This model provides an application-specific economic analysis of the conversion of discrete passive components (resistors and capacitors) to integral passives that are embedded within a printed circuit board. The model performs three basic analyses: 1) Board size analysis is used to determine board sizes, layer counts, and the number of boards that can be fabricated on a panel; 2) Panel fabrication cost modeling including a cost of ownership model is used to determine the impact of throughput changes associated with fabricating integral passive panels; and 3) Assembly modeling is used to determine the cost of assembling all discrete components, and their associated inspection and rework.
- *Liquid Crystal Display: Performance and Reliability* - Display technology is changing at an ever increasing pace. New developments focused towards optimizing power, size, weight, performance and cost are revolutionizing the display industry. The flat panel display market is projected to be around $30 billion worldwide in 2003, of which 86% is expected to be liquid crystal displays. Furthermore active matrix LCDs are projected to be the dominant LCD technology in the coming years. Apart from consumer electronics, increasing use of LCDs in critical applications like defense, avionics and automobiles has evoked the need to understand the reliability of LCD devices. This web handbook is part of this effort to bring together all the scattered data on LCD reliability at one place for the benefit of CALCE consortium members.
- *Long Term Non-Operating Reliability of Electronic Products* - Electronics can experience a range of environments subsequent to manufacture and prior to disposal. Non-operating electronics do not necessarily experience benign environments. The potential environmental stresses on non-operating electronics can be natural, such as those due to climatic conditions, or can be induced by humans. This book examines non-operating electronics reliability issues, outlining and discussing storage conditions, the stresses that can arise in these conditions, and the failure mechanisms that can cause a failure.
- *Microelectronic Defects Database* - The Microelectronic Defects Database (MDD) is a guide to understanding defects and their impact on microelectronics reliability. It allows the user to analyze a failure, to find the root cause defects, or to examine a defect and determine what failures it can cause. To facilitate defect identification and failure analysis, detailed diagrams and high magnification pictures taken with a wide variety of analysis techniques are provided. The philosophy behind this webbook is rooted in the physics-of-failure approach to microelectronics reliability assessment. This webbook can be used to answer the following questions: What defects, environmental, and test or screen loads are the reliability drivers for the device? What magnitudes of defects should be allowed to pass the screens? and, What is the correlation between the defect magnitudes and the operational life?
- *Moisture Diffusion and Corrosion in Electronics* - This webbook provides tutorials, bibliographies, and research work associated with moisture diffusion and corrosion in electronic systems. Moisture ingress into electronic assemblies can have many deleterious effects. In plastic encapsulated microelectronics (PEMs), moisture can cause or attribute to reliability problems such as popcorning, cracking, delamination and corrosion of the

metalization at the die surface. Moisture in printed wiring boards can lead to corrosion, oxidation, and dendritic growth. Corrosion can cause degradation in electrical and mechanical performance of the electronic systems and, eventually, opens or shorts.

- *Plastic Encapsulated Microelectronics (PEM), (including, PEM Encyclopedia, and PEM Bibliography*)- An interactive guide including a webbook, a bibliography, and online movies, provides a state of current technology and guidelines for use, manufacturing, and purchasing of Plastic Encapsulated Microcircuits (PEMs). The webbook presents the science and technology behind PEMs. The advantages of using plastic packages, and the state of the current technology are discussed. A perspective on future trends in plastic encapsulation, especially on chip technology, packaging, design, materials selection, manufacturing processes, device integration and application-specific reliability is included. Also included is a bibliography of a wide range of critical publications in the fields of PEM manufacture, use, and reliability.
- *Power Electronics Failure Mechanisms Database* - An interactive guide providing information on the performance, reliability, and application of power electronic devices. Covers the history, relative performance, appropriate power/frequency regime, and failure mechanisms for a wide range of devices including Metal Oxide Semiconductor Field Effect Transistors (MOSFET), Insulated Gate Bipolar Transistor (IGBT), MOS-Controlled Thyristor (MCT), Bipolar Junction Transistor (BJT), and Gate Turn-Off (GTO).
- *Printed Wiring Board (PWB) Manufacturing* - From calculators to the control panel on the space shuttle, printed wiring assemblies (PWA's) are prominent in today's technological world. Where are they made? How are they made? How are they tested? The answers to these questions and more are in this webbook. Discover the manufacturing and assembly process of PWB's and companies that make this process work.
- *Quality Conformance and Qualification of Microelectronic Packages and Interconnects* - This webbook provides a science-based approach to developing a reliability assessment program for microelectronic packages including failure mechanism identification and modeling. This webbook also discusses failure mechanisms identification and modeling for each of the major package and interconnect elements.
- *Root Cause Identification for Failure in PWBs* - The purpose of failure analysis is to determine the root-cause of what, why, how, and where products can fail. Expert systems, which use decision trees and material data to create solutions to complex problems, can provide users with improved problem-solving capabilities without the expense of additional employees or facilities. This expert system for failure analysis, developed by the CALCE Research Center, provides designers, manufacturers, and users of electronic products a powerful tool in identification and corrective/preventive actions. At this time, our expert system is set up only for failures at the printed wiring board, but will soon include all possible failure mechanisms and defects that can occur in electronic products and systems.
- *Microsensor Technology Review for Life-Consumption Monitoring* – This webbook provides a discussion of the state of microsensor technology and its relevance to life-consumption monitoring. Sensors for a wide range of measurements have been reviewed, including acoustic emissions, angular acceleration, angular rate, linear rate, displacement, pressure, temperature, humidity, chemicals, touch, infrared radiation, fluidic sensors, and remote powering and sensing. Typical applications for each category of sensor are discussed, including the manufacturing and sensing technology, a discussion of the general sensor area, the state of research and commercialization of the sensors, general performance capabilities and limitations, physical properties of the sensors, commercial availability, and a summary table detailing sensor research groups and suppliers, along with critical parameters for specific sensors. Sensors, both in development and on the market, have been cataloged.

CALCE Publications – Over 400 searchable published articles and book chapters

In addition to the resources available on the CALCE Web Site, Consortium members can attend the biannual CALCE Consortium Technical Review and Planning Meetings. Participate on the CALCE Consortium Industrial Advisory Board, and receive Member discounts on CALCE Center Lab Services.

3. How can I justify the cost and the benefits of membership in the CALCE Consortium?

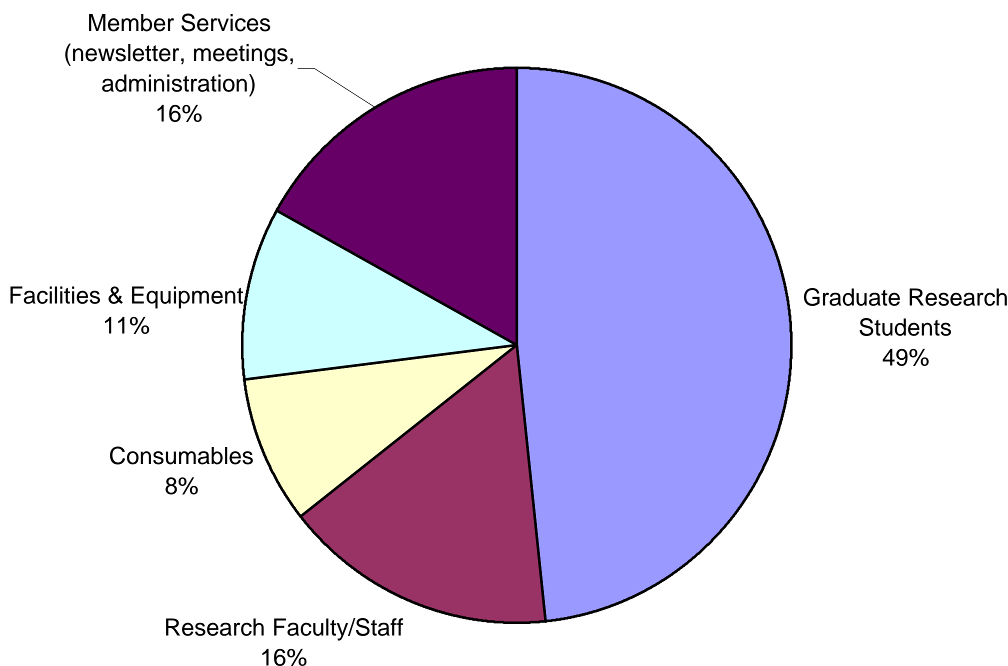
CALCE Consortium members can best determine the means by which the CALCE Consortium can serve them. The manner in which the members wish to avail themselves of the CALCE Consortium benefits will determine the level of benefit they will gain. However, over the years most CALCE Consortium members have reported benefiting significantly from the investment they have made from their CALCE Consortium Membership.

A Return On Investment (ROI) Calculator has been developed to assist organizations in estimating the cost benefit of being a CALCE Consortium Member. The ROI Calculator can be found on the CALCE Web Site at

http://www.calce.umd.edu/ROI_Calculator

4. How is the CALCE EPSC Consortium Membership Fee Used?

CALCE EPSC Consortium Membership Fee is used to fund research and to maintain and support a resource and knowledge base for CALCE EPSC Consortium Members. CALCE Consortium Projects are developed by CALCE Center investigators in coordination with CALCE Consortium Member organizations. Site license fees are used to support the administration, maintenance, and development of CALCE Center resources. A breakdown of how Consortium fees are used is provided below and it is based on the review of expenditures over the past year. Since the below chart represents spending cross Consortium funds, it also represents a typical cost breakdown for a Consortium Project.



5. What are the costs involved in running a CALCE EPSC Consortium project?

Projects are equally funded through a fix budget that is established by the Director of the CALCE Center each year based on the anticipated level of Consortium funding. Investigators use their project budgets to pay for their time, graduate students, project consumables and equipment charges. Equipment is shared between CALCE Consortium projects and the CALCE Electronic Products and Systems Center.

The salary, benefits and tuition of graduate students working on Consortium projects are paid by membership fees of the CALCE Consortium. The state and federal government provide no funding to support graduate students and research assistants, but the cost of graduate students is fixed by the State of Maryland.

The State of Maryland pays for approximately 7 months of salary for most CALCE faculty. The remaining 5 months are financed from faculty research activities. Some of the membership dues go towards this expenditure.

The State of Maryland does not pay for research or support staff.

6. How are CALCE Consortium Project Developed?

Consortium projects are focused on the identification and development of technologies, methodologies, and guidelines for **assessing, mitigating, and managing the risks** associated with the design, manufacture and fielding of electronic products and systems. Consortium project generally fall into one of the following three categories:

- Failure Identification and Reliability Modeling
- Environment and Operational Characterization of Electronic Products
- Risk-informed Technology Insertion Methodologies

The schedule for Consortium Project development is provided below:

- CALCE Consortium candidate projects statements provided by Consortium members to CALCE staff (due Feb 01)
- Post project proposals on website (March 1, 01)
- Present "Green Book[1]" at CALCE Consortium Spring Planning Meeting
- Solicit and review feedback from interest survey[2] (April 1, 01)
- Update project proposals on CALCE Web Site (April 01)
- Send out a "last request" for project comments[3] (July 01)
- Post 2002 projects on website (Sept 18)
- Provide "Green Book" for the Fall Planning Meeting

1. Green Book is a bound book of project proposals that is provided to members at CALCE Consortium Planning Meetings.
2. Interest Survey is compilation of project interest forms that are filled out at CALCE Consortium Planning Meetings.
3. Comments are phone, email, and other communications between Consortium Members and CALCE Research Staff.

CALCE Consortium Projects are developed by CALCE Center investigators in coordination with CALCE Consortium Member organizations.

7. What is the ratio of core research projects to Consortium members?

CALCE Center investigators get a fixed budget for each Consortium project. The number of Consortium projects is based on anticipated funding. One measure of anticipated funding is the number of CALCE Consortium members. As such, number of Consortium projects has always been approximately equal to the number of full Consortium members. A determination of the number of Consortium projects that will be conducted on any given year is made by the Director of the CALCE Center based on are review of the operating budget and a projection of anticipated budget for the upcoming year.

8. What are CALCE EPSC Lab Services?

The CALCE Center has technical staff dedicated to performing engineering services for industry. Lab services are generally proprietary activities that include: virtual qualification of electronic hardware, accelerated test planning, accelerated testing, and material measurement. CALCE Consortium members are given a 20% discount on lab services. Lab services are quoted from a fixed cost sheet.

9. Are there any additional funds which support the CALCE Electronic Products and Systems Center?

Many faculty members seek and accept contracts and grants from outside the Consortium to minimize the cost burden to the CALCE Consortium .The costs of such projects (e.g., the students, consumables, overhead, travel) are not billed to the Consortium. Usually, faculty members try to engage in activities synergistic to the center research, and the consortium members benefit from the lessons learned from these projects. However, some of these are proprietary to the sponsors of these projects and those results are not available to the Consortium.