Thermal Packaging – The Inward Migration

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Brief Thermal Packaging History

DARPA Thermal Management Technologies – Current
- Microtechnologies for Air Cooled Exchangers (MACE)
- Thermal Ground Plane (TGP)
- Nano Thermal Interface Materials (NTI)
- Active Cooling Module (ACM)

DARPA Thermal Management Technologies – Future
- Near Junction Thermal Transport
- Limitations of Remote Cooling
- Towards a New Paradigm ??

Discussion
IBM Air-Cooled Mainframes – 1950’s/1960’s

IBM Mark I Mainframe (1950’s)

IBM System 360; SLT Chips: 1964
History of Thermal Packaging
"The Inward Migration"- an Uncompleted Journey

HVAC Era: 1945-1975
- ENIAC, IBM Mainframes, Telephone switching equipment
- Vacuum tubes and early solid-state transistors
- **Goal: Remove heated air from room/rack/cabinet**

Rack Cooling Era: 1975-1985
- DIP’s and SMT’s on PCB’s
- PCB’s in Card Cages
- **Goal: Maximize natural and forced convection cooling in racks**
History of Thermal Packaging
"The Inward Migration"- an Uncompleted Journey

- Maturation of bipolar devices: ~5W Chips, ~300W MCM’s
- Honeywell, IBM, CDC, Hitachi, NEX, Fujitsu mainframes/supers
- **Goal:** Gain control over the local “coldplate,” “cold bar” temperature

Enhanced Air Cooling Era: 1985-2000
- Thermally-engineered heat sinks for CMOS microprocessors
- Miniaturized servers create Data Center cooling challenge
- **Goals:**
  - *Reduce “case-to-air” resistance for chip package*
  - *Improve Data Center thermal management*
CDC Refrigerated Computers 7600 + Cyber 201/203 1971-1983

- Pioneering refrigeration cooled mainframe
- Refrigerant channels under large PCB’s, later Water cooled PCB’s

http://www.nasm.si.edu/research/dsh/artifacts/GC-CDC3800.htm
http://www.cisl.ucar.edu/computers/gallery/cdc/7600.jsp
IBM Water-Cooling Technology

IBM TCM Module

IBM 3081
Air-Cooled Computers ~ 1990

- 8CPU
- 470x580x80
- 1600W
- Airflow ~ 3.5 m/s

System control LSI
DC-DC Converter
Memory

Air flow
2000+ Thermal Packaging Confronts the “Triple Threat”

Nanoelectronics Era: 2000 –
GHZ-level CMOS with features below 100 nanometers
Distinct on-chip “hot spots” – silicon/compound semiconductors
Emergence of homogeneous/heterogeneous “chip stacks”

Goals:
Reduce/eliminate on-chip “hot spots”
Overcome internal “stack” resistance

3-Dimensional

High Power

Hot Spots

q" hot spot = 500W/cm², 2x2mm; q" avg = 50W/cm², 40x40mm
MMIC On-Chip Hot Spot

Thermal Simulation of GaN MMIC SiC die (380 μm thick) attached to 2-part (closed channel) copper cooler with 50 μm of Sn-3.5Ag

Calame, et al., IEEE Transactions on Components and Packaging Technologies, Vol. 28 Issue 4, pp. 797-809, 2005
Heat Flux Challenge

- Chip Hot Spots
- Ballistic entry
- Nuclear blast
- Reentry from earth orbit
- Rocket motor case
- Solar Flux On Earth’s surface
- On Sun’s surface

Heat Flux (W/cm$^2$) vs. Temperature (K)
### 3D Packaging Configurations

<table>
<thead>
<tr>
<th>Technology &amp; z-Interconnect</th>
<th>Module</th>
<th>Application</th>
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</thead>
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<tr>
<td><strong>Die Stacking (ChipPAC)</strong></td>
<td></td>
<td>▶ Memory</td>
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<tr>
<td>Wire Bond</td>
<td></td>
<td>▶ ASIC + Memory</td>
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<tr>
<td><strong>Die Stacking (ChipPAC)</strong></td>
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<td>▶ ASIC + other</td>
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<tr>
<td>Flip Chip</td>
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<tr>
<td><strong>Package Stacking (Amkor)</strong></td>
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<tr>
<td>Solder Ball</td>
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<tr>
<td><strong>Folded Stacking (Tessera)</strong></td>
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<td>▶ Memory</td>
</tr>
<tr>
<td>Substrate + Solder Ball</td>
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<td>▶ ASIC + Memory</td>
</tr>
</tbody>
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(Dereje Agonafer and Bahgat Sammakia, InterPACK'05)
Heat Density Challenge

- Chip Stack
- Liquid Metal nuclear reactor
- Mercury Vapor lamp
- Light-water nuclear reactor
- Cray-3 Module
- SX-3 Module
- IBM TCM Module
- Electric stove
- Home light bulb
- Halogen bulb
- Human brain

Heat Density (W/cm³) vs. Temperature (K)
Task Areas:

Thermal Ground Plane (TGP): Nanostructured wicks and cases for 2-phase vapor chambers
Microtechnologies for Air-Cooled Exchangers (MACE): Active surfaces/jets for enhanced heat sinks
Nano-Thermal Interfaces (NTI): Engineered, reworkable nanostructures for low resistivity TIMs
Active Cooling Modules (ACM): High COP coolers using novel TE materials/refrigeration concepts
Near-Junction Thermal Transport (NJTT): Active and passive technologies for cooling PA junction

Goal: To deliver transformative thermal management technology that will reduce or remove thermal limitations on DoD platforms
<table>
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<th>Year</th>
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**Thermal Management Technologies (TMT) Overview**

- **Thermal Conductivity**: >20,000 W/mK
- **Operational at**: >10g
- **>4x improvement in thermal resistance**
- **>3x improvement in energy efficiency**
- **>8x improvement in thermal resistance**
- **Reworkable at T<170C**
- **7X better energy efficiency**
- **100W device**
- **3x improvement in RF output power**
- **< 100 microns from junction**

**Motor Blower Spiral Fin-Diffuser Active Reeds**

_Distribution Statement A, Approved For Public Release, Distribution Unlimited_
Thermal Management Technologies (TMT) Microtechnologies for Air-Cooled Exchangers (MACE) Performance

- **Thermacore**: 3D vapor chamber, vibrating elements
- **UTRC**: Integrated blower/heat sink with optimized fin geometry
- **Raytheon**: Micro/Macro Fin; Synthetic jets
- **MIT**: 3D vapor chamber; fan/fin integration
- **Honeywell**: Jet-driven entrainment

![Diagram](image)

**Base Area (cm²)**

- **MACE 1**
- **MACE 2**
- **MACE 3**
- **MACE 4**
- **MACE 5**

**Thermal Resistivity (K·cm²/W)**

- **Alpha Novatech**
- **Wakefield**
- **Aavid**
- **Radian**

3/17/2012

Distribution Statement A, Approved For Public Release, Distribution Unlimited
Thermal Management Technologies (TMT)
Thermal Ground Plane (TGP) Performance

Original Phase 3 Goals:
>20,000 W/mK, <1 mm

- **U Colorado**: flexible/conformal case with Cu nanomesh wick
- **UC Berkeley**: two phase flow with coherent porous silicon wick
- **UC Santa Barbara**: large scale titanium TGP
- **UCLA**: metallic powder + post biporous wick
- **Teledyne**: CNT/Si wick structures
- **Northrop Grumman**: SiC oscillating heat pipe
- **Raytheon**: Patterned CNTs on Cu wick
- **GE**: nanostructured super hydrophobic/philic wick

**DARPA**

**UCP**: Center for High Performance Computing

**NSEC**: National Science Foundation's Engineering Research Center

**CTA**: Center for Thermal Analysis

**MCS**: Materials Crosscutting Security

**GraTech**: Graphite Technologies

**Sp3 Diamond Tech**: Sp3 Diamond Technologies

**Momentive**: Momentive Performance Materials

**ACT**: Advanced Cooling Technologies

**Celsia**: Celsia Technologies

**MinTEQ**: Minimum Total Equivalent Cooling

**Pure Copper**: 401

**Graphite**

**Diamond**

**Vapor Chambers**

**Current TGP**

**Effective Thermal Conductivity, W/mK**

**Thickness, mm**

**TGP Orientation**: horizontal

**Distribution Statement A, Approved For Public Release, Distribution Unlimited**
NTI performance versus commercial TIMs (9/2011)

Thickness, mm

Thermal Resistance, cm² K/W

- Experimental Arctic Silver 5
- Experimental TC-5022
- Experimental G-751
- Theoretical Indalloy 121
- Theoretical Indium

Performer 1 (Sn62)
Performer 3
Performer 4
Performer 1 (indium)
Performer 2
Performer 3
Performer 4

Phase 2 Goal
Phase 3 Goal

Commercial TIM data courtesy of:
D. Altman (Raytheon)
Y. Zhao (Teledyne)
Thermal Management Technologies (TMT)
NTI Recent Progress

- GE NTI team has demonstrated thermal resistance significantly outperforming the Phase 1 metric of 0.070 cm\(^2\)-C/W
- \(~15\%\) of samples better than the Phase 3 metric of 0.010 cm\(^2\)-C/W

Spring radius is controlled by substrate rotation speed

Patterned GLAD, 3 turns, diameter=250nm, 550 nm pitch

GLAD Process

GLAD fabrication by Micralyne (Alberta, CA)
Thermal Management Technologies (TMT)
NTI Recent Progress

Teledyne – graphite/solder laminate

Novel TIM – laminated layers of aligned graphite films and solder.
- Thermal resistivity = 0.04 cm² C/W on 300 µm thick prototypes
- Thermal resistivity = 0.01 cm² C/W on 125 µm thick prototypes
**Vision:** Provide localized thermal management within the device substrate to increase Output Power from WBG PA’s by >3x

**High Thermal Conductivity Over-layer for Heat Removal from Topside of Devices**
- High thermal conductivity in deposited material
- Conformal coverage with no gaps

**Embedded Thermal Vias**
- Micro-machined vias within ~1 micron of junction
- High thermal conductivity conformal fill materials
- Low coupling resistance for junction-to-thermal via, thermal via-to-heat sink

**High Thermal Conductivity Substrates**
- Integrate lattice-mismatched heat spreaders
- Eliminate thermal interface resistance
- Match coefficient of thermal expansion of electronic material

**Anisotropic Heat Transport**
- Efficient nanoscale phonon channel
- Long LO phonon lifetime (3ps)
- Extremely low electrical contact resistance

**Active Liquid Cooling**
- Eliminate impact on device electrical properties due to time varying dielectric constant of liquid

**Substrate**
- Drain
- Gate
- Source
- ~ 1mm thickness

**Electronic Junction**

**DARPA**

**Thermal Management Technologies (TMT) Near-Junction Thermal Transport (NJTT)**

Vision: Provide localized thermal management within the device substrate to increase Output Power from WBG PA’s by >3x
**GaN-on-Substrate Transistors**

- Common substrates: Sapphire, Si, and SiC
- Typical Dimensions
  - Gate (Finger) pitch: 10 - 50 µm
  - Gate (Finger) length: 50 - 200 µm
  - Gate (Finger) width: 0.25 - 1 µm
- Linear Power: 40-50 W/mm possible, 1-10 W/mm in practice
- Linear Heat Dissipation: 0.5-5 W/mm in practice

**GaN-on-SiC Device Heating**

- Conditions: 5W/mm, 150 µm x 0.5 µm gate; 50 µm gate pitch
  - Heat Flux: \( q'' \) PA average \( \sim 100 \text{ W/mm}^2 \)
    - \( q'' \) peak (channel) \( \sim 10 \text{ kW/mm}^2 \)
  - Temperatures: \( T_{\text{junction}} = 150 \text{ °C} - 200 \text{ °C} \)
    - \( \Delta T \) Near Junction Rise = 80K

Heat rejection to a remote fluid involves thermal conduction and spreading in substrates across multiple material interfaces with associated thermal parasitics.

Incapable of effectively limiting the device “junction” temperature rise

Can not selectively target the thermally-critical devices

Accounts for a large fraction of the weight and volume of advanced high power electronics, lasers, and computer systems

Stymies attempts to port advanced systems to small form-factor applications

Remote cooling frustrates attempts to reach CSWaP targets
Towards a New Thermal Packaging Paradigm

- Challenge: Complete the Inward Migration of Thermal Packaging
- Extract heat directly from device, chip, and package where generated
- Place thermal management on an equal footing with functional design and power delivery
- Successful implementation of embedded thermal management will:
  - Allow electronic systems to reach material, electrical and/or optical limits
  - Reduce CSWaP for comparable performance
  - Lead the way to integrated, intelligent, and holistic system co-design